SEMICONDUCTOR DEVICE HAVING BUMP ELECTRODES

Background of the Invention

1 Field of the Invention

This invention relates to the electronic assembly technology and more specifically to the semiconductor device having bump electrodes.

2. Description of the Related Art

As electronic devices have become more and more smaller and thinner, the velocity and the complexity of IC chips have become more and more higher. Accordingly, a need has arisen for higher package efficiency. Demand for miniaturization is the primary catalyst driving the usage of advanced packages such as tape carrier package (TCP). TCP is commonly used in the manufacture of liquid crystal display modules. These liquid crystal displays provide the advantages of low cost, high reliability, high-density storage, light weight, and low power consumption. The tape carrier package generally comprises a semiconductor device having bump electrodes. Moreover, the semiconductor device having bump electrodes are also used in chip on glass (COG) technology, which permits direct attachment of chips to a glass substrate.

Bumping method typically comprises the steps of (a) forming under bump metallurgy (UBM) on bonding pads of the semiconductor device, and (b) forming metal bumps on the UBM. Usually, gold is chosen as the material of metal bumps for meeting the requirements of proceeding TCP or COG process. Typically, the UBM adapted for gold bumps consists of three metal layers, including: (a) adhesion layer (formed of Al or Cr) for providing a good adhesion to Al pad and passivation layer; (b) barrier layer (formed of Cu, Pd or Pt) for preventing chip contact pad and metal bump from reacting with each other to generate an intermetallic compound (which is harmful to the reliability of the chips); and (c) wetting layer (formed of Au).

Fig. 1 is a cross sectional view of a conventional semiconductor device 10 having a bump electrode. An aluminum contact pad 11 is formed on a substrate 12 of a semiconductor integrated circuit. The substrate 12 comprises a plurality of resistances, capacities and inductors of input/output units （I/Os）. A passivation film 13, serving as an insulation film, is formed on the entire surface of the substrate 12. A passivation opening section which is formed at a predetermined position, is formed to expose the aluminum contact pad 11. The

semiconductor device 10 has a UBM 14 consisting of three metal layers, including: (a) chromium layer 14a (as the adhesion layer); (b) copper layer 14b (as the barrier layer); and (c) gold layer 14c (as the wetting layer). After the multilayers for the UBM are formed over the entire surface of the substrate 12, a gold bump 15 is plated on the UBM 14 through photoresist application and its patterning. Finally, the UBM layers that are not covered by the gold bump 15 are etched away.

Fig. 2 is a cross sectional view of another conventional semiconductor device 20 having a bump electrode. The semiconductor device 10 has a UBM 24 consisting of three metal layers, including: (a) titanium layer 24a (as the adhesion layer); (b) palladium layer 24b (as the barrier layer); and (c) gold layer 24c (as the wetting layer).

Fig. 3 is a cross sectional view of still another conventional semiconductor device 30 having a bump electrode. The semiconductor device 30 has a UBM 34 consisting of three metal layers, including: (a) titanium layer 34a (as the adhesion layer); (b) platinum layer 34b (as the barrier layer); and (c) gold layer 34c (as the wetting layer).

However, all of the prior art UBMs mentioned above comprise a gold layer under the gold bump. Thus, a gold target is required for used in the sputtering process thereby increasing the cost. Furthermore, when an etching process is conducted for patterning the gold layer of the UBM, the gold bump is also etched during the process thereby creating undesired effect on the bump height uniformity and the uniformity of bump surface roughness, which, in turn, adversely affect the quality of the gold bump.

The present invention therefore seeks to provide an under bump metallurgy which overcomes, or at least reduces the above-mentioned problems of the prior art, thereby maintaining the uniformity of the gold bumps.

Summary of the Invention

It is a primary object of the present invention to provide a semiconductor device having gold bump electrodes wherein the under bump metallurgy adapted for the bump electrode utilizes a titanium layer as the wetting layer thereby replacing the expensive gold layer and acquiring a better etching selectivity.

It is another object of the present invention to provide a semiconductor device having bump electrodes wherein the under bump metallurgy adapted for the bump electrode utilizes nickel-vanadium layer as the barrier layer to reduce the influence of I/Os on the plating

process of the gold bump, thereby maintaining the bump height uniformity and the uniformity of bump surface roughness.

The semiconductor device having bump electrodes according to the present invention comprises an aluminum contact pad on a substrate wherein at least a portion of the aluminum contact pad is exposed through a dielectric layer on the substrate. An under bump metallurgy (UBM) is formed on the aluminum contact pad. The under bump metallurgy comprises an aluminum layer formed on the exposed portion of the aluminum contact pad, a nickel-vanadium layer formed on the aluminum layer and a titanium layer formed on the nickel-vanadium layer. A gold bump is provided on the UBM over aluminum contact pad so as to form the bump electrode.

The present invention further provides a method for forming a semiconductor device having a bump electrode. The method comprises (a) providing an aluminum contact pad on a semiconductor substrate, at least a portion of the aluminum contact pad being exposed through a dielectric layer on the substrate; (b) forming an aluminum layer on the dielectric layer and the portion of the aluminum contact pad exposed through the dielectric layer; (c) forming a nickel-vanadium layer on the aluminum layer; (d) forming a titanium layer on the nickel-vanadium layer; (e) cleaning the titanium layer with a cleaning medium; (f) selectively plating a gold bump on the titanium layer at a location corresponding to the aluminum contact pad; and (g) etching the aluminum layer, the nickel-vanadium layer and the titanium layer with the gold bump as a mask.

According to the present invention, the UBM of the semiconductor device having bump electrodes comprises an aluminum layer, a nickel-vanadium layer and a titanium layer. Since the nickel-vanadium layer with a lower electrical conductivity is utilized as the barrier layer, the influence imposed by I/Os of the semiconductor device during the plating process of the gold bump is significantly reduced, thereby maintaining the bump height uniformity and the uniformity of bump surface roughness. Furthermore, the UBM of present invention utilizes the titanium layer instead of the expensive gold layer as the adhesion layer to reduce the cost. However, the titanium layer may react with the oxygen in air to form an oxidizing layer on the surface thereof, and the oxidizing layer should be removed before proceeding to the plating process of the gold bump so as to assure a good adhesion between the gold bump and the UBM thereby improving electrical performance.

Brief Description of the Drawings

Other objects, advantages, and novel features of the invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

Fig. 1 is a schematic sectional view of a conventional semiconductor device having a bump electrode;

Fig. 2 is a schematic sectional view of another conventional semiconductor device having a bump electrode;

Fig. 3 is a schematic sectional view of still another conventional semiconductor device having a bump electrode;

Figs. 4 and 5 illustrate in cross-section major steps of fabrication of a semiconductor device having a bump electrode according to a preferred embodiment of the present invention; and

Fig. 6 is a schematic sectional view of a semiconductor device having a bump electrode according to the preferred embodiment of the present invention.

Detailed Description of the Preferred Embodiment

Figs. 4 and 5 illustrate the major steps in the manufacture of a semiconductor device having a bump electrode according to a preferred embodiment of the present invention.

Fig. 4 shows a semiconductor device including a substrate 110, an aluminum contact pad 120, and a dielectric layer such as passivation layer 130. The substrate 110 may comprise a layer of a semiconducting material such as silicon, gallium arsenide, silicon carbide, diamond, or other substrate materials known to those having skill in the art. The passivation layer 130 is preferably a polyimide layer but can alternately be a silicon dioxide layer, a silicon nitride layer, or layers of other passivation materials known to those having skill in the art. As shown, the passivation layer 130 preferably covers the top edge portion of the aluminum contact pad 120 opposite the substrate 110, leaving the central surface portion of the aluminum contact pad 120 exposed from the passivation layer 130. The under bump metallurgy (UBM) 140 of the present invention comprises an aluminum layer 140a formed on the portion of the aluminum contact pad 120 exposed from the passivation layer 130, a nickel-vanadium layer 140b formed on the aluminum layer 140a and a titanium layer 140c formed on the nickel-vanadium layer 140b. The UBM 140 of the present invention chooses

the aluminum layer 140a as the adhesion layer to provide a good adhesion to the aluminum contact pad 120 and the passivation layer 130. Furthermore, the UBM 140 utilizes the titanium layer 140c instead of the conventional gold layer as a wetting layer; hence, the manufacturing cost is reduced by utilizing a cheaper titanium target in the sputtering process. The UBM 140 of the present invention is preferably formed by a subtractive process.

As shown in Fig. 4, the aluminum layer 140a, the nickel-vanadium layer 140b and the titanium layer 140c are respectively sputtered on the passivation layer 130 and the exposed portions of the aluminum contact pad 120.

Fig. 5 shows a gold bump 150 being disposed on the UBM 140 over the aluminum contact pad 120 to act as a bump electrode. Specifically, the gold bump 150 is formed by the following steps: (a) Application of a photoresist 160 on UBM 140 and its patterning to form opening at a location corresponding to the pad 120; and (b) Electrodeposition of gold on the resist opening section to form the gold bump 150. Typically, the gold bump 150 comprises at least about 90 weight percentage of Au.

Since TiO or TiO_2 may be formed on the surface of the titanium layer due to the oxidation of titanium, it is preferable to remove the TiO or TiO_2 with a cleaning medium before the electrodeposition of the gold bump so as to assure a good adhesion between the gold bump and the UBM thereby improving electrical performance. Preferably, the cleaning medium is HCl.

Furthermore, the UBM 140 of the present invention is characterized by utilizing the nickel-vanadium layer 140b as a barrier layer. Since the electrical conductivity of the nickel-vanadium is lower than copper, palladium, or platinum, the influence imposed by I/Os of the semiconductor substrate 110 on the current density during the plating process of the gold bump is significantly reduced, thereby maintaining the bump height uniformity and the uniformity of bump surface roughness.

Referring to Fig. 5, after the gold bump 150 is formed on the UBM 140, the UBM 140 is etched with the plated gold bump 150 as a mask thereby obtaining the semiconductor device 100 having a bump electrode as shown in Fig. 6. The titanium layer 140c of UBM 140 can be selectively etched by acidic solution such as HCl. Since the gold bump 150 is quite resistant to HCl etching agent, the gold bump is substantially unaffected during the etching process of UBM 140 thereby obtaining a good uniformity in bump height and bump surface roughness. This significantly enhances the yield of proceeding processes.

Although the invention has been explained in relation to its preferred embodiment, it is to be understood that many other possible modifications and variations can be made without departing from the spirit and scope of the invention as hereinafter claimed.